REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19															
REV STATUS OF SHEETS			REV																	
			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Joseph A. Kerby	**DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444**
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, CMOS, PROGRAMMABLE SKEW CLOCK BUFFER, MONOLITHIC SILICON
	APPROVED BY Monica L. Poelking	
	DRAWING APPROVAL DATE 94-09-13	SIZE **A** / CAGE CODE **67268** / **5962-93112**
AMSC N/A	REVISION LEVEL	SHEET 1 OF 19

DESC FORM 193
JUL 91

5962-E270-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q, and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	93112	01	M	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_______________ _______________/
V
Drawing number

1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Skew error
01	7B992	Programmable skew clock buffer	0.7 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Desciptive designator	Terminals	Package style
X	CQCC1-N32	32	Leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883(see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CCN}, V_{CCQ})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to +7.0 V dc
Output current into outputs (low) (I_{OL})	64 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	911 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CCN}, V_{CCQ})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	0 V dc to V_{CCQ}
Output voltage range (V_{OUT})	0.0V dc to V_{CCN}
High level input voltage range (V_{IH}, V_{IHH}):	
V_{IH}	V_{CCQ} - 1.35 V dc to V_{CCQ} 4/
V_{IHH}	V_{CCQ} - 1.00 V dc to V_{CCQ} 5/ 6/
Mid level input voltage range (V_{IMM})	V_{CCQ}/2 ±500 mV dc 5/
Low level input voltage range (V_{IL}, V_{ILL}):	
V_{IL}	-0.0 V dc to 1.35 V dc 4/
V_{ILL}	0.0 V dc to 1.0 V dc 5/ 6/
Case operating temperature (T_C)	-55°C to +125°C
Input rise or fall time (t_r, t_f):	
($0.2V_{CC}$ to $0.8V_{CC}$: $0.8V_{CC}$ to $0.2V_{CC}$)	0 to 3 ns
Maximum high level output current (I_{OH})	-40 mA
Maximum low level output current (I_{OL})	+46 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ Unless otherwise specified the values listed above shall apply over the full V_{CCN}, V_{CCQ} and T_C recommended operating range. For the absolute maximum parameters, the limits shall apply over the full specified V_{CCN}, V_{CCQ} ranges and case temperature range of -55°C to +125°C.

4/ This voltage range applies to the REF and FB inputs only.

5/ This voltage range applies to the TEST, FS, and mFn inputs only. These inputs are normally wired to V_{CCQ} or GND or left unconnected, (actual threshold voltages vary as a percentage of V_{CCQ}), internal termination resistors hold unconnected inputs at V_{CCQ}/2. If these inputs are switched the function and timing of the outputs may glitch and the phase-lock-loop (PLL) may require an additional T_{LOCK} time before all table I limits are acheived.

6/ Negative undershoots of -2.0 V dc are allowed with a pulse width < 20 ns.

7/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration management.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Frequency range and t_U calculation and programmable skew configuration. The frequency range and t_U calculation and programmable skew configuration shall be as specified on figure 2.

3.2.4 Block diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 132 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

   (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

   (2) $T_A = +125^\circ C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except that interim electrical tests prior to burn in are optional at the discretion of the manufacturer for device class M.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55^\circ C \leq T_C \leq +125^\circ C$ $+4.5\ V \leq V_{CCN}, V_{CCQ} \leq +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
High level output voltage 3006	V_{OH}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = V_{CC}$ -1.35 V V_{IL} = 1.35 V I_{OH} = -40 mA $V_{CCQ} = V_{CCN}$ = 4.5 V	All	1,2,3	V_{CCN} -0.75		V
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = V_{CC}$ -1.35 V V_{IL} = 1.35 V I_{OL} = 46 mA $V_{CCQ} = V_{CCN}$ = 4.5 V	All	1,2,3		0.45	V
Input leackage current, high, (REF and FB inputs only) 3010	I_{IH}	For input under test $V_{IN} = V_{CCQ}$ $V_{CCN} = V_{CCQ}$ = 5.5 V	All	1,2,3		10.0	µA
Input leakage current, low, (REF and FB inputs only) 3009	I_{IL}	For input under test V_{IN} = 0.4 V $V_{CCN} = V_{CCQ}$ = 5.5 V	All	1,2,3	-500		µA
Input current, high, (test, FS, mFn) 3010	I_{IHH}	For input under test $V_{IN} = V_{CCQ}$ $V_{CCN} = V_{CCQ}$ = 5.5 V	All	1,2,3		200	µA
Input current, mid, (test, FS, mFn) 3010	I_{IMM}	For input under test $V_{IN} = V_{CCQ}/2$ $V_{CCN} = V_{CCQ}$ = 5.0 V	All	1,2,3	-50.0	+50.0	µA
Input current, low, (test, FS, mFn) 3010	I_{ILL}	For input under test V_{IN} = GND $V_{CCN} = V_{CCQ}$ = 5.5 V	All	1,2,3	-200.0		µA
Operating current used by internal circuitry 3005	I_{CCQ}	REF = FB = 0.0 V Test = FS = mFn = open $V_{CCN} = V_{CCQ}$ = 5.5 V I_{OUT} = 0.0 mA	All	1,2,3		90	mA
Output buffer current per output pair 3005	I_{CCN} 4/	Frequency = 50 MHz $V_{CCN} = V_{CCQ}$ = 5.5 V I_{OUT} = 0.0 mA Input selects open FS = 5.5 V, TEST = 0.0 V FB connected to 3Q0	All	4,5,6		19.0	mA
Power dissipation per output pair	P_D 5/		All	4,5,6		104	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55^\circ C \le T_C \le +125^\circ C$ $+4.5 V \le V_{CCN}, V_{CCQ} \le +5.5 V$ unless otherwise specified		Device type	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input capacitance 3012	C_{IN}	REF and FB inputs only frequency = 1 MHz $V_{CCQ} = V_{CCN} = 5.0$ V see 4.4.1b		All	4		10	pF
Functional testing 3014		$V_{IL} = 0.0$ V 6/ verify output V_O $V_{CCQ} = V_{CCN} = V_{IH} = 4.5$ V and 5.5 V See 4.4.1c		All	7,8			
Operating clock frequency	f_{NOM} 7/ 8/	$C_L = 50$ pF $R_1 = R_2 = 100\Omega$ See figure 2	FS = low	All	9,10,11	15	30	MHz
			FS = mid			25	50	
			FS = high			40	50	
REF pulse width, high	t_{RPWH}	$C_L = 50$ pF minimum R1 = R2 = 100Ω See figure 4		All	9,10,11	5.0		ns
REF pulse width, low	t_{RPWL}			All	9,10,11	5.0		ns
Programmable skew unit	t_U			All	9,10,11	9/		
Programmable skew unit error	t_{UE} 10/ 16/			All	9,10,11	-0.7	+0.7	ns
Zero output matched-pair skew (mQ0, mQ1)	t_{SKEWPR} 11/ 12			All	9,10,11		0.25	ns
Zero output skew (all outputs)	t_{SKEW0} 11/ 13/			All	9,10,11		0.75	ns
Output skew (rise - rise, fall - fall, same class outputs)	t_{SKEW1} 11/ 14/			All	9,10,11		1.0	ns
Output skew (rise - fall, nominal-inverted, divided-divided)	t_{SKEW2} 11/ 14/			All	9,10,11		1.5	ns
Output skew (rise - rise, fall - fall, different class outputs)	t_{SKEW3} 11/ 14/			All	9,10,11		1.2	ns

footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55^\circ C \le T_C \le +125^\circ C$ $+4.5\ V \le V_{CCN}, V_{CCQ} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Output skew (rise - fall, nominal - divided, divided - inverted)	t_{SKEW4} 11/ 14/	C_L = 50 pF minimum R1 = R2 = 100Ω See figure 4	All	9, 10, 11		1.7	ns
Device-to-device skew	t_{SKEW5} 11/ 14/		All	9, 10, 11		0.2	ns
Propagation delay, REF rise to FB rise 3005	t_{PD}		All	9, 10, 11	-0.7	+0.7	ns
Output duty cycle variation	t_{ODCV} 17/		All	9, 10, 11	-1.2	+1.2	ns
Output high time, deviation from 50 percent	t_{PWH}	18/ Not shown in figure 4	All	9, 10, 11		5.5	ns
Output low time, deviation from 50 percent	t_{PWL}					5.5	ns
Output rise time	t_{ORISE}	C_L = 50 pF minimum R1 = R2 = 100Ω See figure 4	All	9, 10, 11	0.5	5.0	ns
Output fall time	t_{OFALL}		All	9, 10, 11	0.5	5.0	ns
Phase-locked-loop lock time	t_{LOCK} 19/		All	9, 10, 11		0.5	ms
Cycle-to-cycle output jitter peak-to-peak	t_{JR} 16/		All	9, 10, 11		0.5	%

1/ For tests not listed in the referenced MIL-STD-883 (e.g. I_{OS}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input and output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except during I_{CC} tests, for which the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ I_{ICCN} can be approximated by the following expression:

I_{ICCN} = [(3.5 + .17F) + [((1160 - 2.8F)/Z) + (.0025FC)]N]*1.1.

where:

F = frequency in MHz
C = capacitance load in pF
Z = line impedance in ohms
N = number of loaded outputs (0, 1, or 2)
FC = F x C

5/ The value specified in table I applies to each output pair. Power dissipation can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
P_D = [(19.25 +0.94F) + [((700 - 6F)/Z) + (.017FC)]N] * 1.1.
where variables are defined as in footnote 6. CMOS buffer current and power dissipation are specified at the 50 MHz reference frequency. Testing is done initially and after any design or process changes that affect this parameter; values are guaranteed to the limits given in table I herein.

6/ Functional testing is guaranteed when inputs are conditioned with the worst case input voltage as specified in 1.4 herein.

7/ For all three-level inputs, High = V_{CC}, Mid = open connection, Low = GND. Internal termination circuitry holds an unconnected input to $V_{CC}/2$. When the FS pin is selected high the REF input must not transition upon power-up until V_{CC} has reached 4.3 V.

8/ The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator. Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see figure 2). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB in undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.

9/ See figure 2 herein, Frequency range select and t_U calculation.

10/ t_{UE} is a measure of the timing error from t_U as calculated in figure 2 herein (Frequency range select and t_U calculation). The major contributors to the error include output edge variations, cross talk, and load-induced variations between package pins and between signal lines external to the chip. t_{UE} is not cumulative across multiple t_U delays.

11/ Skew is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50 pF and terminated with 50Ω to $V_{CC}/2$.

12/ t_{SKEWPR} is defined as the skew between a pair of outputs (mQ0 and mQ1) when all eight outputs are selected for $0t_U$.

13/ t_{SKEW0} is defined as the skew between all eight outputs when all are selected for $0t_U$. Other outputs are divided or inverted but not shifted.

14/ For the purpose of this specification, there are three classes of outputs, defined as follows: nominal (multiple of t_U delay), inverted (4Q0 and 4Q1 only with 4F0 and 4F1 = High), and divided (3Qn and 4Qn only in divide-by-2 or divide-by-4 mode).

15/ t_{SKEW5} is the output-to-output skew between the outputs used as the FB input of two or more devices operating under the same conditions (e.g., V_{CC} level, ambient temperature, air flow.) The maximum variation between two parts is t_{SKEW5} plus the skews associated with each part.

16/ Testing is done initially and after any design or process changes that affect this parameter; values are guaranteed to the limits given in table I herein.

17/ t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} parameters.

18/ Tested with outputs loaded with 50 pF; devices are terminated through 50Ω to $V_{CC}/2$. t_{PWH} is measured at $0.8V_{CC}$; t_{PWL} is measured at $0.2V_{CC}$.

19/ t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	REF	17	FB
2	V_{CCQ}	18	V_{CCN}
3	FS	19	2Q1
4	3F0	20	2Q0
5	3F1	21	GND
6	4F0	22	GND
7	4F1	23	1Q1
8	V_{CCQ}	24	1Q0
9	V_{CCN}	25	V_{CCN}
10	4Q1	26	1F0
11	4Q0	27	1F1
12	GND	28	GND
13	GND	29	2F0
14	3Q1	30	2F1
15	3Q0	31	TEST
16	V_{CCN}	32	GND

Terminal symbol descriptions		
Terminal symbol	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	Phase-locked loop feedback input (typically connected to one of the eight inputs.)
FS	I	Three-state frequency range select (see figure 2 herein.)
mFn (m = 1 to 4, n = 0 to 1)	I	Three-state function select inputs.
TEST	I	Test mode select. In normal operation, this input will be wired to GND. See 6.5
mQn, mQn (m = 1 to 4) (n = 0 or 1)	O	Outputs. Three-state input pairs (i.e. 1F1, 2F1, ...) are matched with output pairs (i.e. 1Q1, 2Q1, ...)
V_{CCN}	PWR	Power supply for output drives.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

FIGURE 1. Terminal connections.

Frequency range select and t_U calculation 1/

FS 2/	f_{NOM} (MHz)		$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate frequency at which t_U = 1.0 ns
	Min	Max		
Low	15	30	44	22.7 MHz
Mid	25	50	26	38.5 MHz
High	40	80 3/	16	62.5 MHz

Programmable skew configurations 1/ 4/

Function selects		Output functions		
mF1	mF0	1Qy, 2Qy	3Qy	4Qy
Low	Low	$-4t_U$	Divide by 2	Divide by 2
Low	Mid	$-3t_U$	$-6t_U$	$-6t_U$
Low	High	$-2t_U$	$-4t_U$	$-4t_U$
Mid	Low	$-1t_U$	$-2t_U$	$-2t_U$
Mid	Mid	$0t_U$	$0t_U$	$0t_U$
Mid	High	$+1t_U$	$+2t_U$	$+2t_U$
High	Low	$+2t_U$	$+4t_U$	$+4t_U$
High	Mid	$+3t_U$	$+6t_U$	$+6t_U$
High	High	$+4t_U$	Divide by 4	Inverted

NOTES:

1/ For all three-state inputs (FS and mFn), High indicates a connection to V_{CC}, Mid indicates an open connection, and Low indicates a connection to GND. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.

2/ The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time unit generator (see figure 3 herein). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.

3/ The value, 80 MHz in the frequency range select and t_U calculation, is a reference value only and not to be construed as a maximum frequency device type 01 can achieve.

4/ The skew select matrix (see figure 3 herein) is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select inputs (mF0, mF1). This table shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

FIGURE 2. Frequency range and t_U calculation and programmable skew configuration.

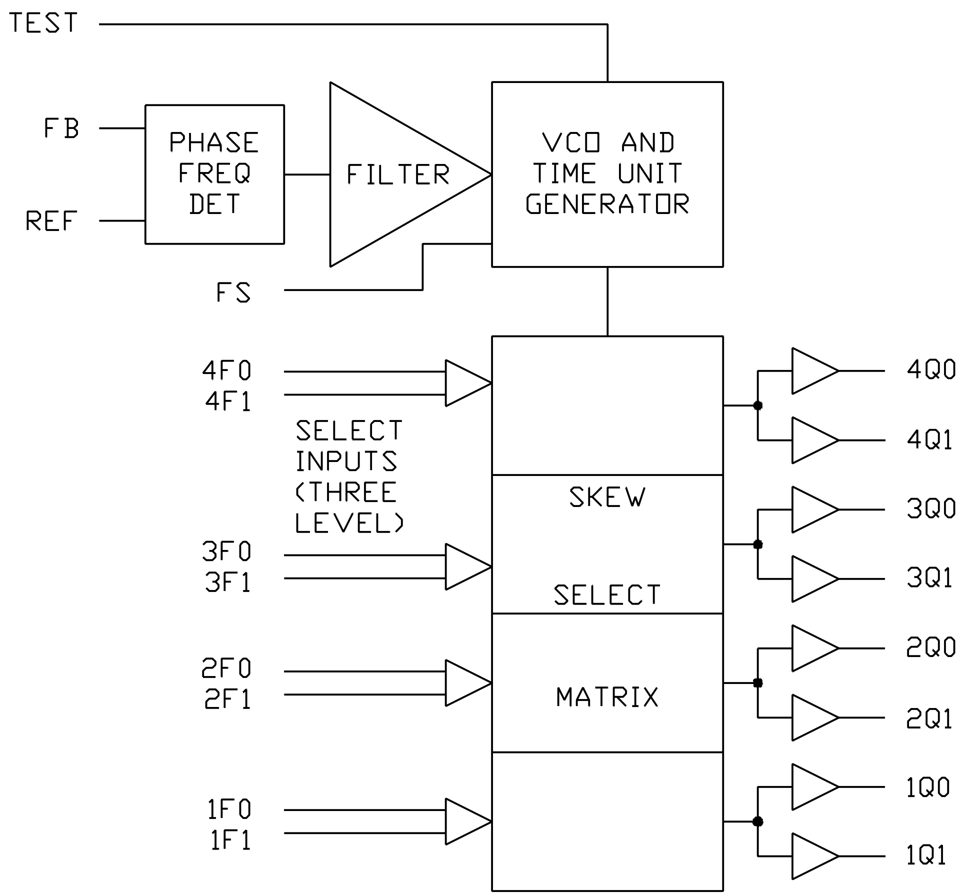


FIGURE 3. Logic diagram.

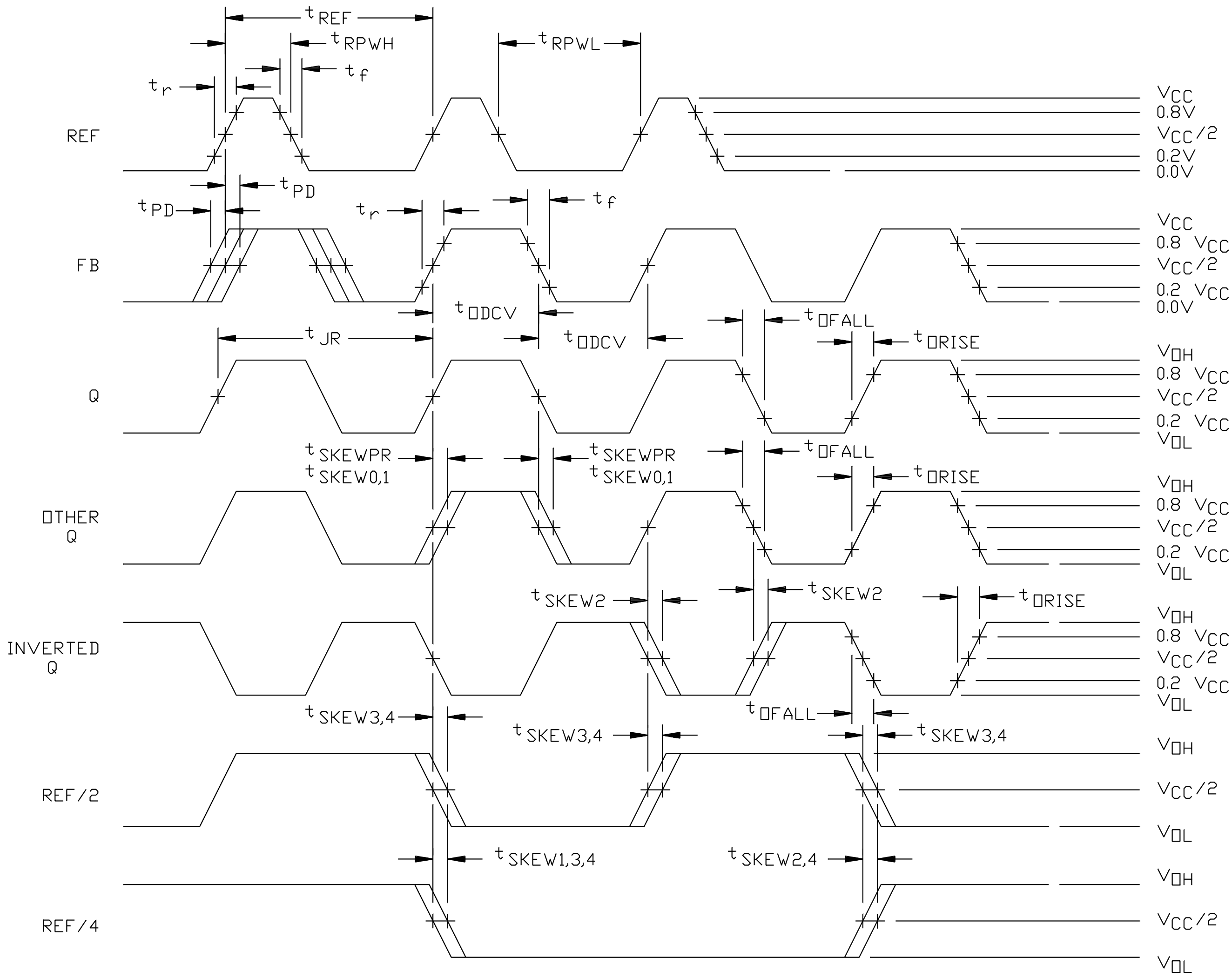
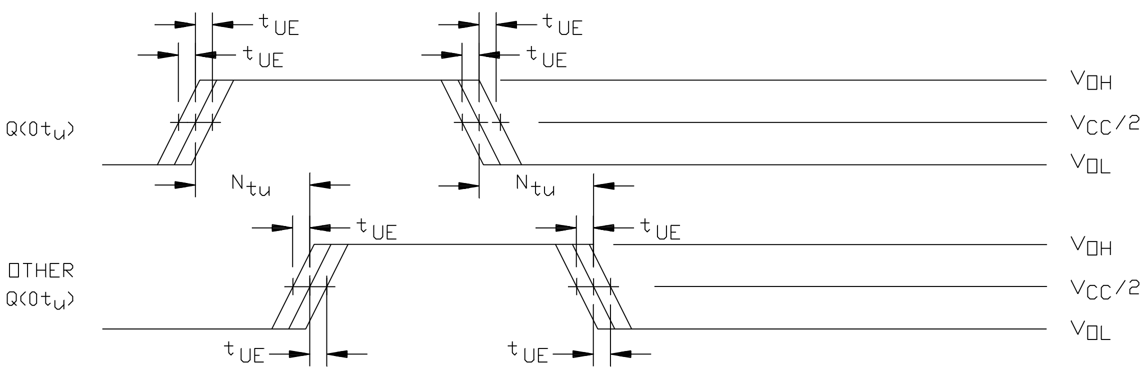
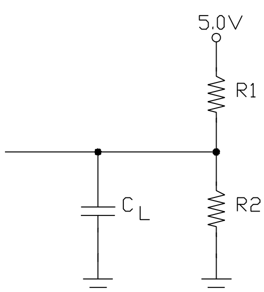
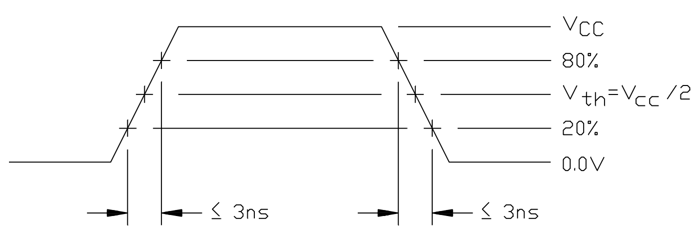


FIGURE 4. Switching waveforms and test circuit.



Output load circuit **AC test conditions**





NOTE:
R1 = 100Ω; R2 = 100Ω; C_L = 50 pF, including fixture and probe capacitance (minimum values).

4. Switching waveforms and test circuit - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. C_{IN} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN} test all applicable pins on five devices with zero failures.

   For C_{IN} a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN} tests. The device manufacturer may then test one device functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. $T_A = +125^\circ C$, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end point electrical parameters (see 4.4)	1, 2, 3, 4	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end point electrical parameters (see 4.4)	1, 2, 3, 4	1, 2, 3	1, 2, 3
Group E end point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 4 (I_{CCN} only).
2/ PDA applies to subgroups 1, 4 (I_{CCN} only) and 7 .

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

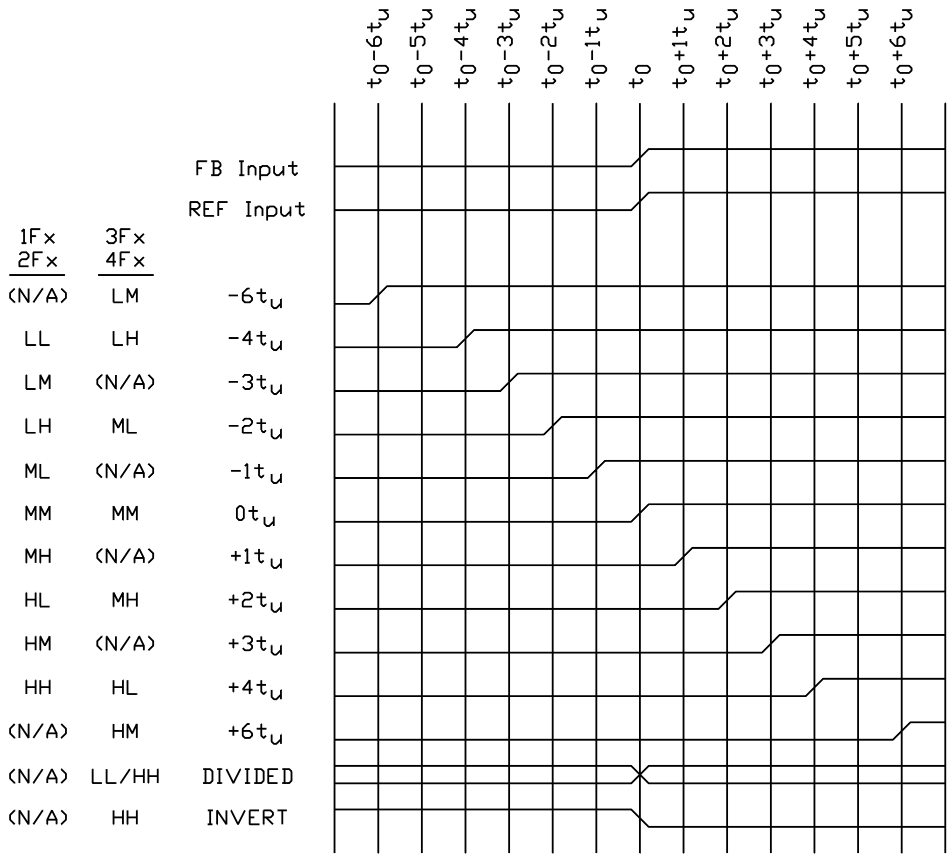
6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

C_{IN} . . . . Input terminal capacitance.
GND . . . . Ground zero voltage potential.
I_{CC} . . . . Supply current.
I_I . . . . Input current.
T_C . . . . Case temperature.
V_{CC} . . . . Positive supply voltage (5.0 V).
REF . . . . Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB . . . . PLL feedback input (typically connected to one of the eight outputs).
FS . . . . Three-level frequency range select.
1F0, 1F1 . . . . Three-level function select inputs for output pair 1 (1Q0, 1Q1).
2F0, 2F1 . . . . Three-level function select inputs for output pair 2 (2Q0, 2Q1).
3F0, 3F1 . . . . Three-level function select inputs for output pair 3 (3Q0, 3Q1).
4F0, 4F1 . . . . Three-level function select inputs for output pair 4 (4Q0, 4Q1).
TEST . . . . Three-level select
V_{CCN} . . . . Power supply for output drivers.
V_{CCQ} . . . . Power supply for internal circuitry.



Test Mode:

The test input is a three-level input. In normal operation, the FB pin is connected to ground, allowing device type 01 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied low through a 100Ω resistor. This will allow an external tester to change the state of these pins).

If the test input is forced to its mid or high state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (test tied low), all outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-09-13

Approved sources of supply for SMD 5962-93112 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9311201MXX	65786	CY7B992-7LMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134-1599